CLAIMS

1. An adaptive method of prefetching data blocks from an input/output device, said method comprising:

predicting the address of each read operation reading a data block from said input/output device, the prediction based on the address of the immediately preceding read operation from said input/output device;

tracking, for each said read operation, whether each said read operation reads a data block from the same address of the input/output device predicted for said read operation; and

prefetching a data block for a read operation from said input/output device in accordance with the state of a state machine, the state of the state machine depending upon whether immediately preceding read operations read a block data from the same address of the input/output device predicted for said read operations.

2. The adaptive method of prefetching data blocks recited in claim 1, wherein the address predicted for each read operation has a defined relationship to the address of the immediately preceding read operation and, if prefetched, the data block prefetched is at the predicted address.

3. The adaptive method of prefetching data blocks recited in claim 2, wherein the address predicted for each read operation is the next address after the address of the immediately preceding read operation and any data block prefetched is the data block at the next address after the address of the immediately preceding read operation.

4. The adaptive method of prefetching data blocks recited in claim 1, wherein the state machine has a succession of states, the state of the state machine increasing by one state each time a read operation reads a data block from the same address predicted for said read operation and decreasing by one state each time a read operation does not read a data block from the same address predicted for said read operation.

5. The adaptive method of prefetching data blocks recited in claim 4, wherein the state machine has a succession of four states, the bottom two states in which prefetching is not carried out and the top two states in which prefetching is carried out, the state next to the top state being the initial state of the state machine.

6. An adaptive prefetch circuit prefetching data blocks to be read from an input/output device, said adaptive prefetch circuit comprising:

a memory prefetch unit, said memory prefetch unit receiving a read request signal, an address of a first read operation of an input/output device and a length signal, predicting the address of each read operation subsequent to the first read operation reading a data block from said input/output device, the prediction based on the address of the immediately preceding read operation from said input/output device, and tracking, for each said subsequent read operation, whether each said read operation reads a data block from the same address of the input/output device predicted for said read operation; and

a state machine, the state of the state machine depending upon whether immediately preceding read operations read a data block from the same address of the input/output device predicted for said read operations,

wherein the memory prefetch unit prefetches a data block for a read operation subsequent to said first read operation from said input/output device in accordance with the state of said state machine.

7. The adaptive prefetch circuit recited in claim 6, wherein the address predicted for each read operation has a defined relationship to the address of the immediately preceding read operation and, if prefetched, the data block prefetched is at the predicted address.

8. The adaptive prefetch circuit recited in claim 7, wherein the address predicted for each read operation is the next address after the address of the immediately preceding read operation and any data block prefetched is the data block at the next address after the address of the immediately preceding read operation.

9. The adaptive prefetch circuit recited in claim 6, wherein the state machine has a succession of states, the state of the state machine increasing by one state each time a read operation reads a block data from the same address predicted for said read operation and decreasing by one state each time a read operation does not read a block data from the same address predicted for said read operation.

10. The adaptive prefetch circuit recited in claim 9, wherein the state machine has a succession of four states, the bottom two states in which prefetching is not carried out and the top two states in which prefetching is carried out, the state next to the top state being the initial state of the state machine.

11. A server comprising:

at least one processor;

random access memory;

a plurality of input/output devices;

an input/output control circuit; said input/output control circuit controlling the transfer of data blocks between said at least one processor, said random access memory and said plurality of input/output devices; and

at least one adaptive prefetch circuit prefetching a data block to be read from said plurality of input/output devices, said adaptive prefetch circuit comprising:

a memory prefetch unit, said memory prefetch unit receiving a read request signal, an address of a first read operation of one of said plurality of input/output devices and a length signal, predicting the address of each read operation reading a block data from said one input/output device subsequent to the first read operation, the prediction based on the address of the immediately preceding read operation from said one input/output device, and tracking, for each said subsequent read operation, whether each said read operation reads a data block from the same address of said one input/output device predicted for said read operation; and

a state machine, the state of the state machine depending upon whether immediately preceding read operations read a data block from

the same address of said one input/output device predicted for said read operations,

wherein the memory prefetch unit prefetches a block data for a read operation subsequent to said first read operation from said input/output device in accordance with the state of said state machine.

12. The server recited in claim 11, further comprising at least one bus connecting said plurality of input/output devices to said input/output control circuit.

13. The server recited in claim 12, further comprising input/output interfaces respectively connecting corresponding ones of said plurality of input/output devices to a bus, said input/output interfaces comprising a bus master for requesting access to said bus.

14. The server recited in claim 13, wherein at least one of said input/output interfaces comprises said at least one adaptive prefetch circuit.

15. The server recited in claim 14, wherein a plurality of separate adaptive prefetch circuits are comprised in respective corresponding input/output interfaces.

16. The server recited in claim 12, wherein said at least one adaptive prefetch circuit is included in said input/output control circuit.

17. The server recited in claim 11, wherein the address predicted for each read operation has a defined relationship to the address of the immediately preceding read operation and, if prefetched, the data block prefetched is at the predicted address.

18. The server recited in claim 17, wherein the address predicted for each read operation is the next address after the address of the immediately preceding read operation and any data block prefetched is the data block at the next address after the address of the immediately preceding read operation.

19. The server recited in claim 16, wherein the state machine has a succession of states, the state of the state machine increasing by one state each time a read operation reads a block data from the same address predicted for said read operation and decreasing by one state each time a read operation does not read a data block from the same address predicted for said read operation.

20. The adaptive prefetch circuit recited in claim 19, wherein the state machine has a succession of four states, the bottom two states in which prefetching is not carried out and the top two states in which prefetching is carried out, the state next to the top state being the initial state of the state machine.